# Nelson Campos

Electrical Engineer, MSc.


nelsoncscampos

sistenix.com

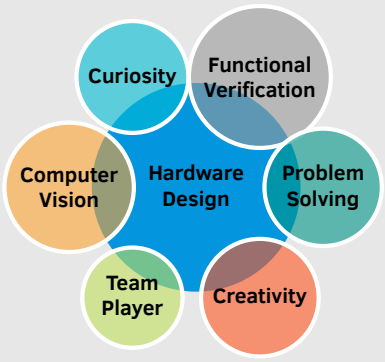
nelson@ieee.org

/in/nelsoncsc

nelsoncsc


## Skills

### Overview




### Programming

0 → 5

Matlab • Python • LaTeX

Verilog • SystemVerilog • UVM

C • C++ • SystemC

## Selected Projects

**RECURSIVE_FFT** - Fixed Point Recursive FFT.
**ISP UVM** - A Framework for Design and Verification of Image Processing Applications using UVM.
**SV-MATH** - Reusable math modules (multiplication, division, square root and logarithm) in SystemVerilog.
**SV-IMAGE** - Reusable image processing modules in SystemVerilog.
**FIR FILTER** - FIR Filter Generation and Audio Processing in Altera DE2.

## Education

2015 - 2017 **MSc., Electrical Engineering** (GPA: 9.08/10.0) Federal University of Campina Grande

2008 - 2015 **BEng., Electrical Engineering** (GPA: 8.09/10.0) Federal University of Campina Grande

## Research

2015 - 2017 **Masters Degree, Graduate Research Assistant** Federal University of Campina Grande

**Thesis**: A Framework for Design and Validation of Face Detection Systems

- Proposed a a framework for design (implementation of IP-Cores) and validation (functional verification using UVM) of image processing and computer vision applications.
- Defined evaluation metrics to validate a TLM face detection system based on Viola Jones algorithm within the proposed framework.

## Publications

**A Framework for Design and Validation of Face Detection Systems (link)**
**Nelson Campos**, Heron Monteiro, Alisson Brito, Antonio M. N. Lima, Elmar Melcher, Marcos Morais
*IEEE CHILECON 2017, Pucón, Chile.*

**Energy Consumption Measurement of an FPGA Full-HD Video Processing Platform**
Heron A. Monteiro, **Nelson C. S. Campos**, Jozias P. Oliveira, Antonio Marcus N. Lima, Alisson V. Brito, Elmar U. K. Melcher
*WCAS 2017, Fortaleza, Brazil.*

**A 4-MHz parameterized Logarithm-Square Root IP-Core (link)**
**Nelson Campos**, Roberto Costa, Elton Costa, Gutemberg Junior, Elmar Melcher
*IPSOC 2016, Grenoble, France.*

**Plataforma Didática para Simulação do Controle de Frequência em um Sistema Elétrico de Potência aplicando o Droop Speed Control**
Jonatas R. Kinas, Rayan L. B. França, **Nelson C. de S. Campos**, Nicolau K. L. Dantas, J. S. da Rocha Neto (Senior member IEEE), Maurício B. de R. Correa (Member IEEE)
*COBENGE 2016, Natal, Brazil.*

## Experience

Sep 2016 - May 2017 **Junior Engineer** Technological Park of Paraiba

- Production of training material in microelectronics for the Project of Excellence in Microelectronics at SONY/PEM/UFCG.

Nov 2013 - Sep 2017 **IP-Core Developer & Verification Engineer** Dedicated Architectures Laboratory

- Experience in Design (SystemVerilog) and Verification (SystemC/UVM) and prototyping in FPGA.
- Development of IP-Cores for a Power Line Communication Modem using S-FSK modulation for data transmission in narrowband.
- Study and design of modules for a Speech Recognition System.
- Verification of a computer vision platform for face detection.